ISL97656 SEPIC for $3V_{IN}$ to $12V_{IN}$ to $3.3V_{OUT}$ at 1A Application

Introduction

There are several applications where one needs to generate a constant output voltage which is right in the middle of the input voltage range. This circuit can easily be implemented by using any boost regulator, as long as it can handle the input voltage range, and the output load current configured in a SEPIC (Single Ended Primary Inductively Coupled) configuration. The SEPIC circuit in Figure 1 is designed for a raid disk application to generate a constant $3.3V_{out}$ to provide power to an FPGA, white LED driver, and EEPROM from an input voltage source that ranges from 3V to 12V by using ISL97656. The ISL97656 is a selectable 640kHz, or 1.2MHz constant switching frequency, high efficiency boost regulator for $2.3V_{IN}$ to $5.5V_{IN}$ applications. It has an internal 120mΩ, 4A power switch which allows over 90% efficiency and has an external compensation pin which allows ceramic capacitors on the output.

Since the input voltage range on the ISL97656 is from 2.3V to 5.5V and the system applications requires input to vary from 3V to 12V, a discrete bias supply is created by using D_2 (3.1V zener) and R_1 (100Ω). This bias supply is only used for start-up, and gets disconnected when the ISL97656 starts regulating 3.3V on the output. When there is no output voltage, Q_1 is off, Q_2 and Q_3 are on, hence, D_2 zener diode generates approximately 3.1V, which supplies input power to the chip. Once the external soft-start capacitor times out, the ISL97656 starts switching at 1.2MHz since the “Freq” pin is grounded and starts regulating 3.3V on the output. At this time, output turns on Q_1 which turns-off Q_2 and Q_3, turning D_2 zener diode off. At this point, the ISL97656 is powered from the output through D_3, Schottky diode. The purpose of disconnecting the zener diode from the circuit by using Q_1, Q_2 and Q_3, is to prevent excessive power loss when the input voltage is 12V. This power loss across the zener diode will translate into poor SEPIC efficiency at load currents of less than 200mA. If output efficiency is not a major concern, then remove R_5, R_6, R_7, Q_1, Q_2, and Q_3 and connect the top side of R_1 directly to the input supply. The bill of material for this evaluation board is listed in Table 1, and the front and back side of this evaluation board is shown in Figures 2 and 3.

Figure 4 shows the ISL97656 efficiency from $12V_{IN}$, and Figure 5 from $3V_{IN}$. It can be seen that the ISL97656 SEPIC circuit is 80+% efficient from $12V_{IN}$ vs. about 75% from $3V_{IN}$. Figure 6 shows the output voltage ripple of 71mV at 0.7A of load current. The output voltage ripple is about 2% and can be further reduced by adding another output capacitor in parallel.

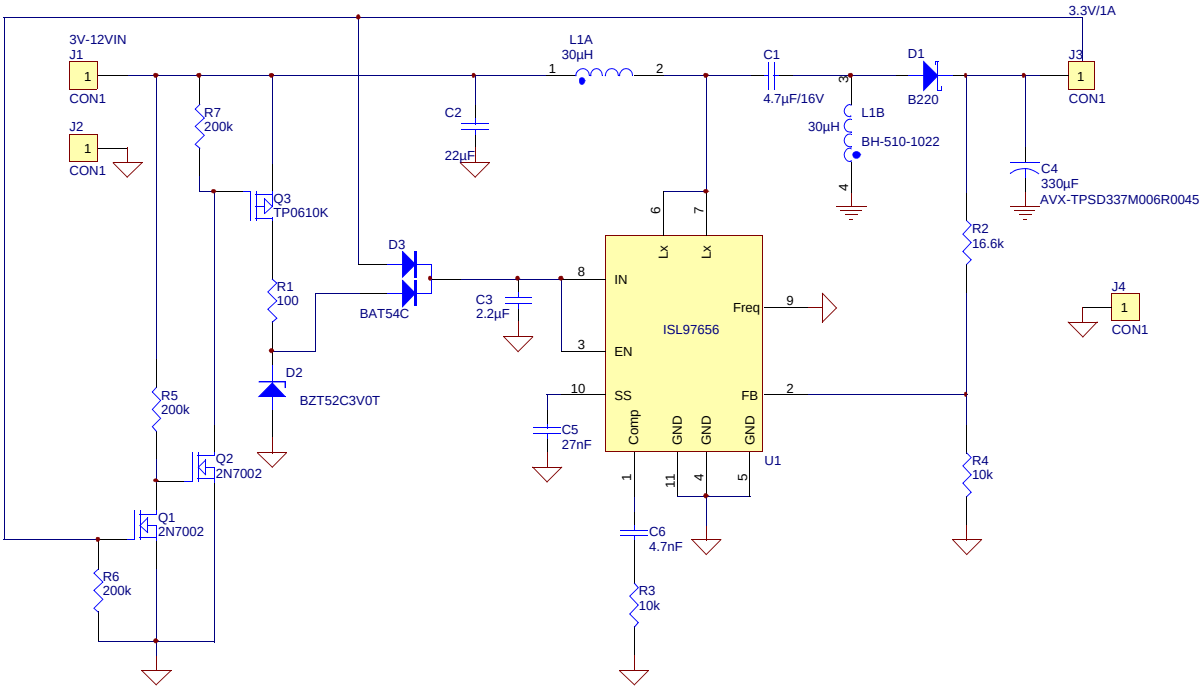

FIGURE 1. ISL97656 SEPIC SCHEMATIC FOR 3V to $12V_{IN}$ TO $3.3V_{OUT}$ AT 1A

TABLE 1. ISL97656 SEPIC BILL OF MATERIAL

PART TYPE	DESIGNATOR
2.2µF	C3
4.7µF/16V	C1
2N7002	Q1
TPK0610K	Q3
2N7002	Q2
10k	R3
4.7nF	C6
10K	R4
16.6k	R2
22µF	C2
27nF	C5
100	R1
200k	R6
200k	R7
200k	R5
330µF	C4
B220	D1
BAT54C	D3
BZT52C3V0T	D2
BH Elect, 510-1022	L1A/B
U1	ISL97656

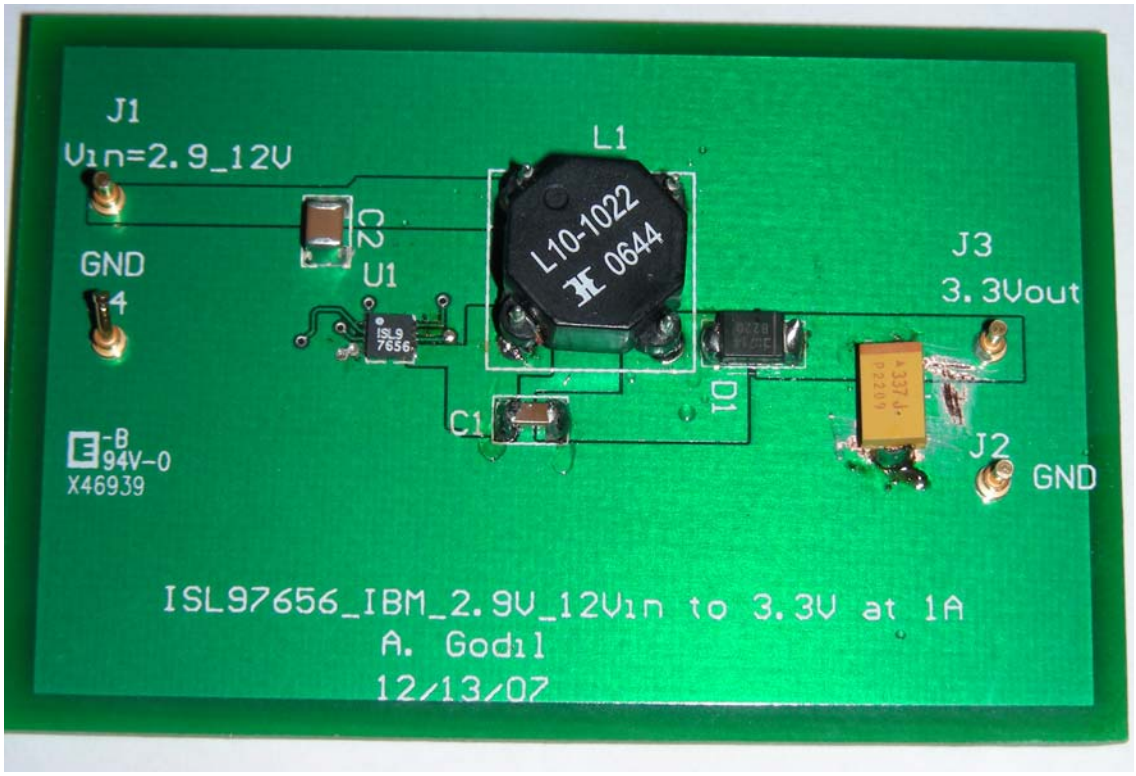

FIGURE 2. ISL97656 SEPIC TEST BOARD – FRONT SIDE

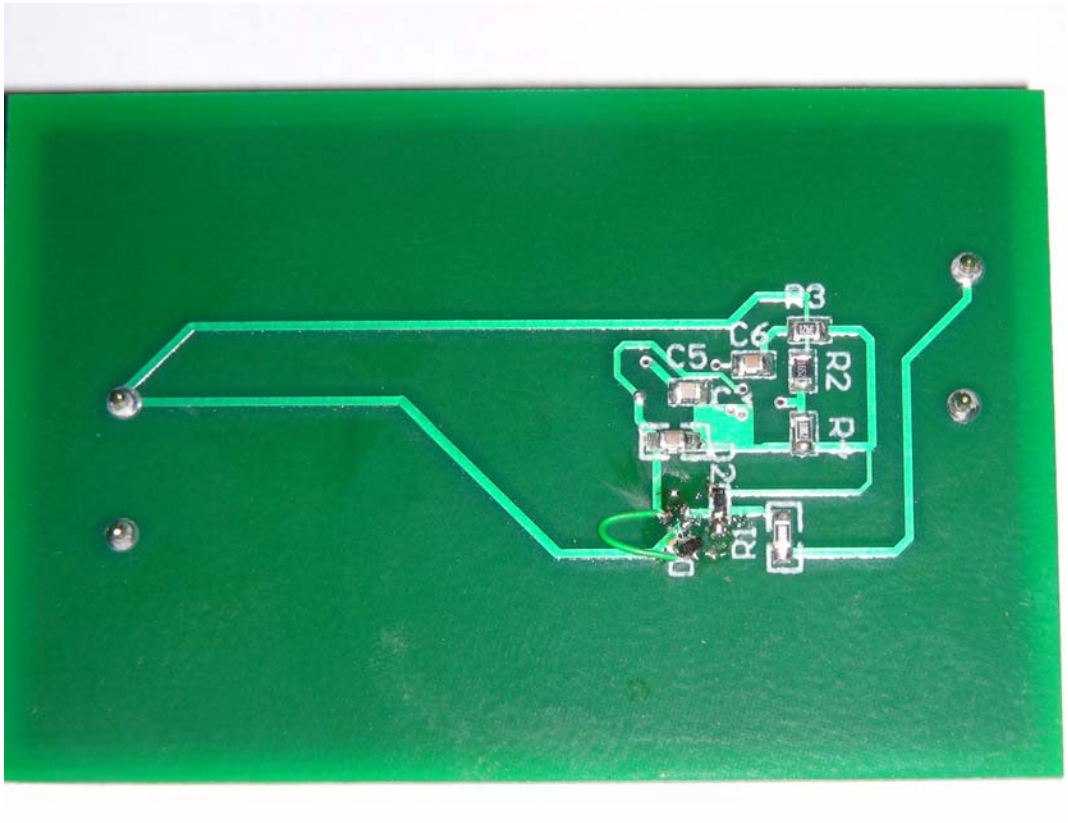

FIGURE 3. ISL97656 SEPIC TEST BOARD – BACK SIDE

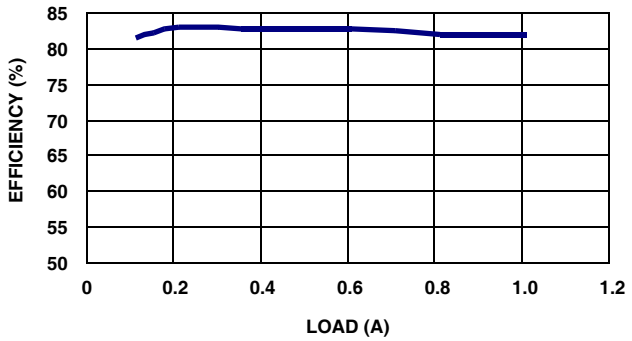

FIGURE 4. ISL97656 SEPIC BOARD EFFICIENCY FROM $12V_{IN}$

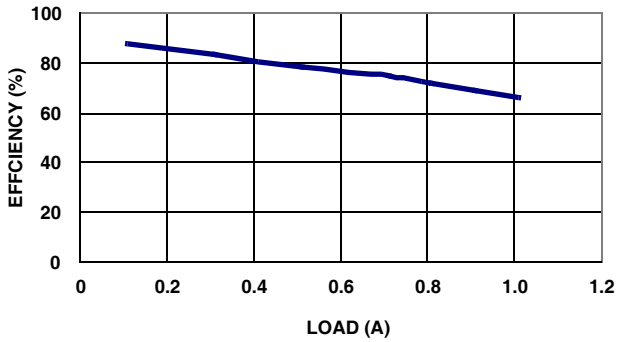

FIGURE 5. ISL97656 SEPIC BOARD EFFICIENCY FROM $3V_{IN}$

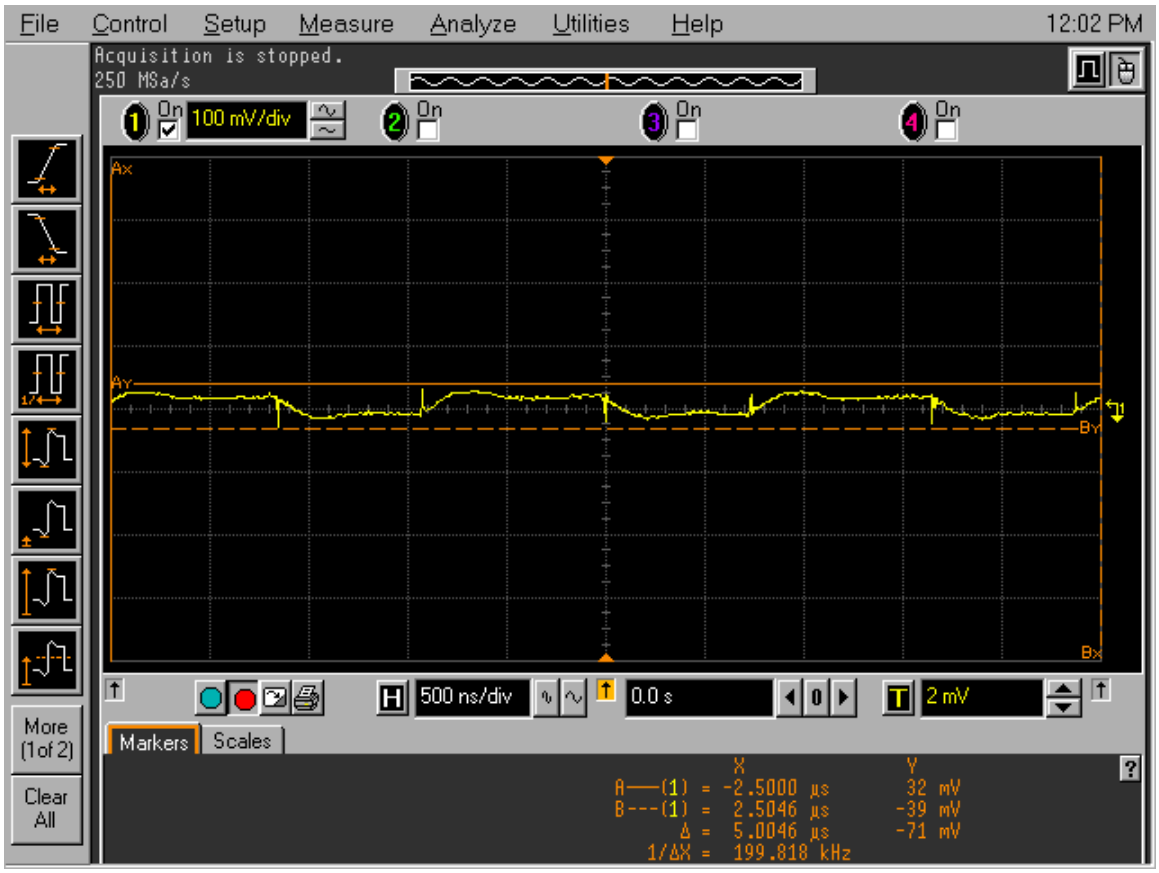

FIGURE 6. ISL97656 SEPIC BOARD OUTPUT VOLTAGE RIPPLE FOR $12V_{IN}$ TO $3.3V_{OUT}$ AT 0.7A